MIPS with Pipelining

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[16:0]

1

**+**

Addr

Data\_in

Wr\_en Data\_out

DATA MEM

Clt5

Clt3

Clt8

Instruction

Ctl2

[16:12]

Ctl7

BT

Opcode

Controller

Ctrl1

[26:22]

[15:0]

[31:27]

[16:12]

[21:17]

Wr\_addr

Wr\_en

Data\_in

REG MEM

NAND

X

+/-

ALU

Addr

Data1

Prog MEM

Addr1 Addr2

Data1

Data2

REG FILE

L\_we

U\_we